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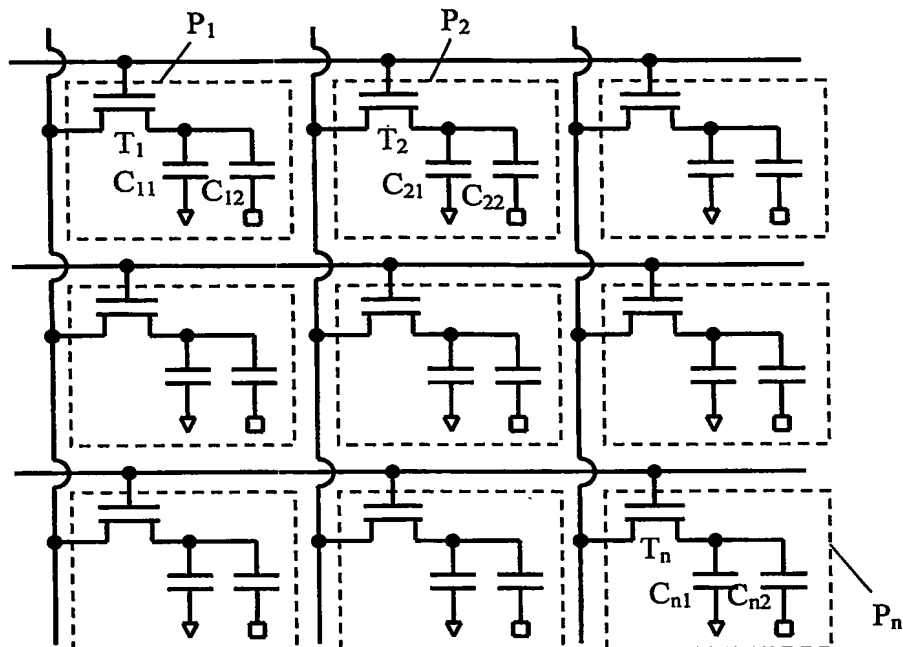


Fig. 1 - Prior Art

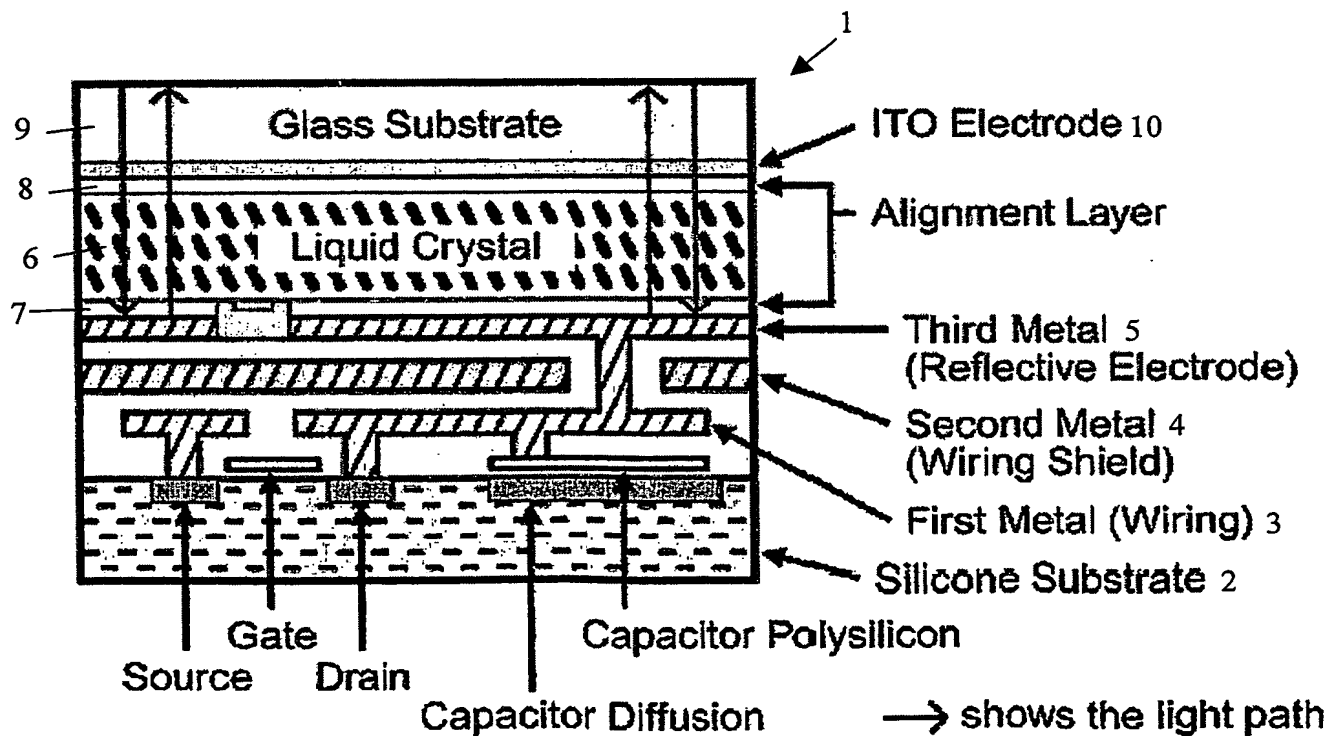


Fig. 2

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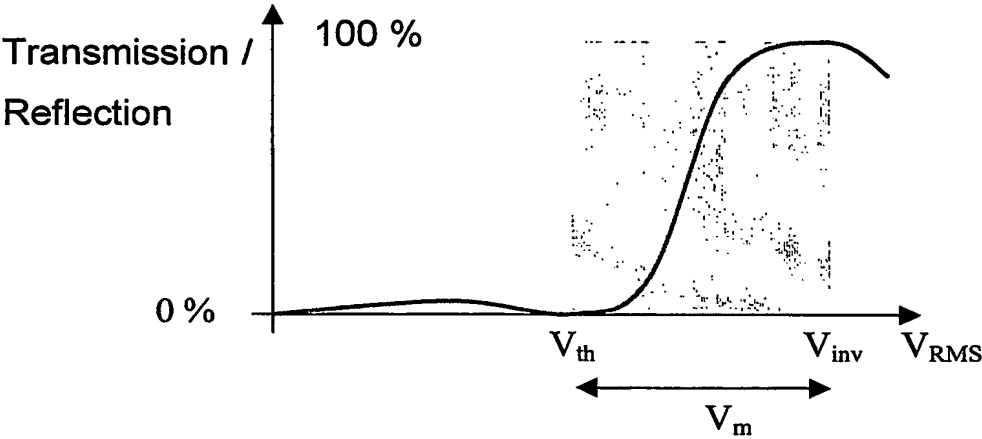


Fig. 3

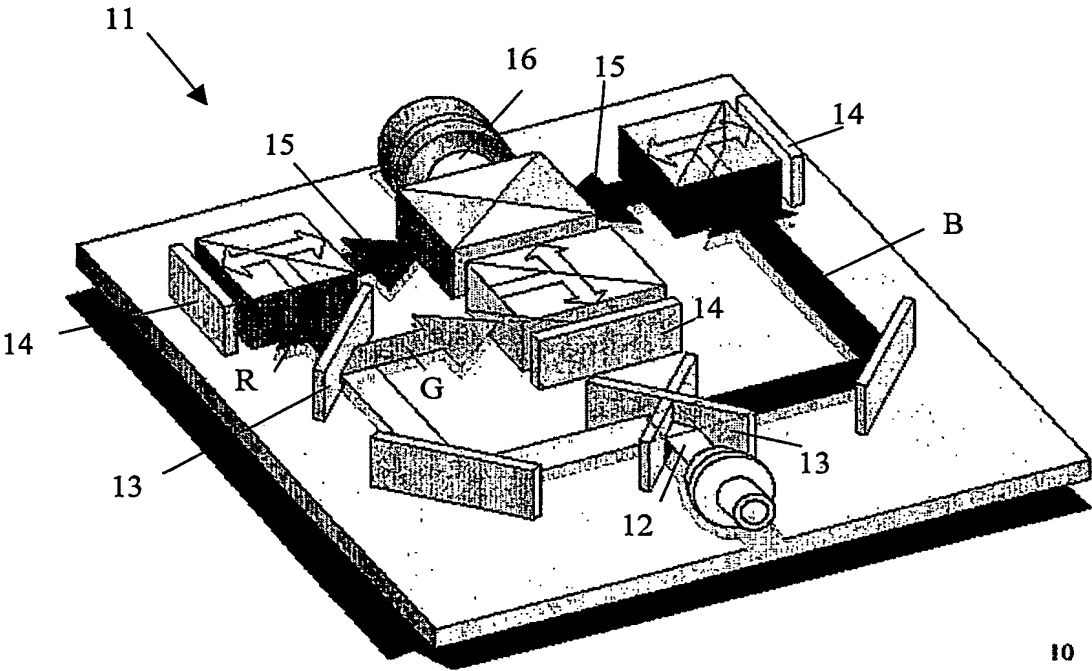


Fig. 4

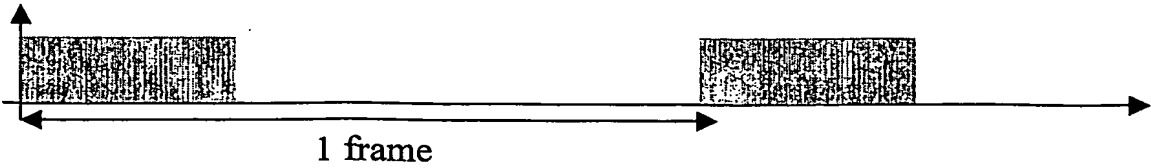


Fig. 5

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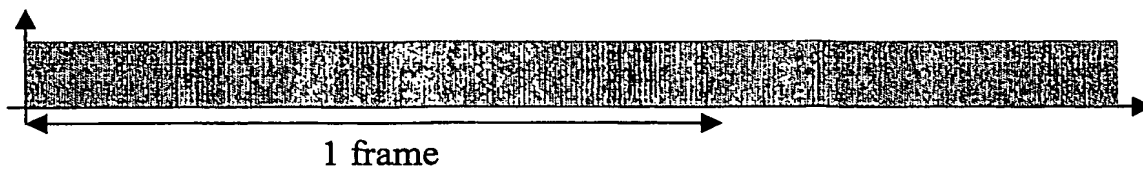


Fig. 6

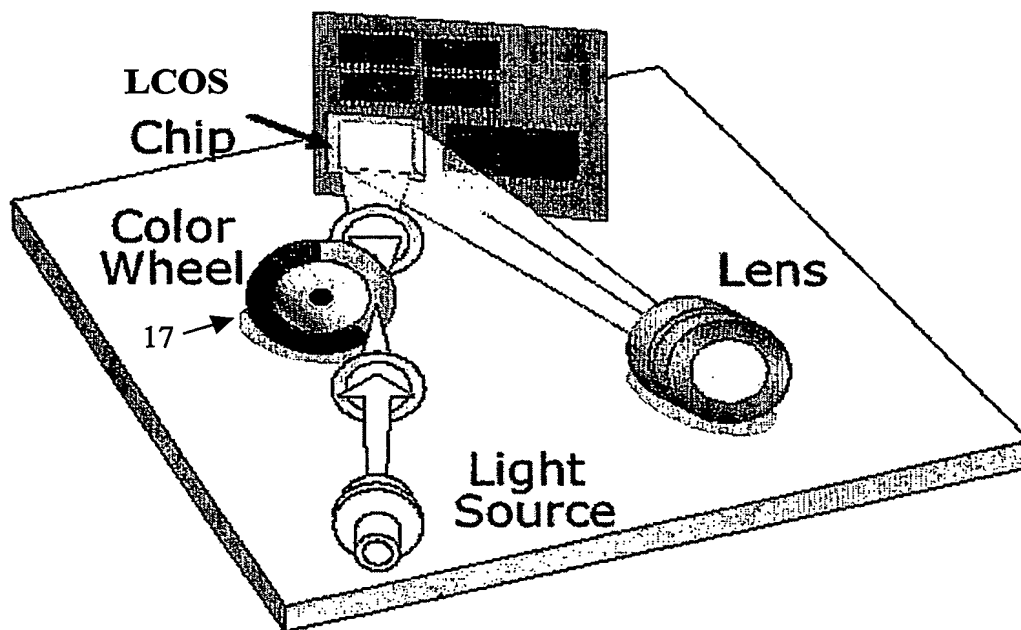


Fig. 7

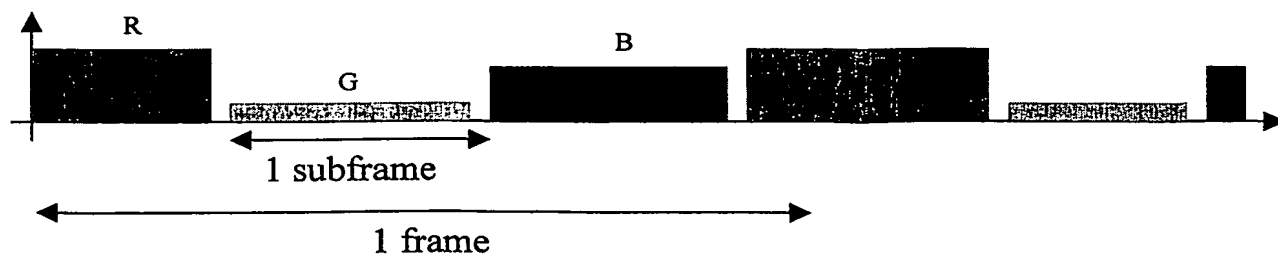


Fig. 8

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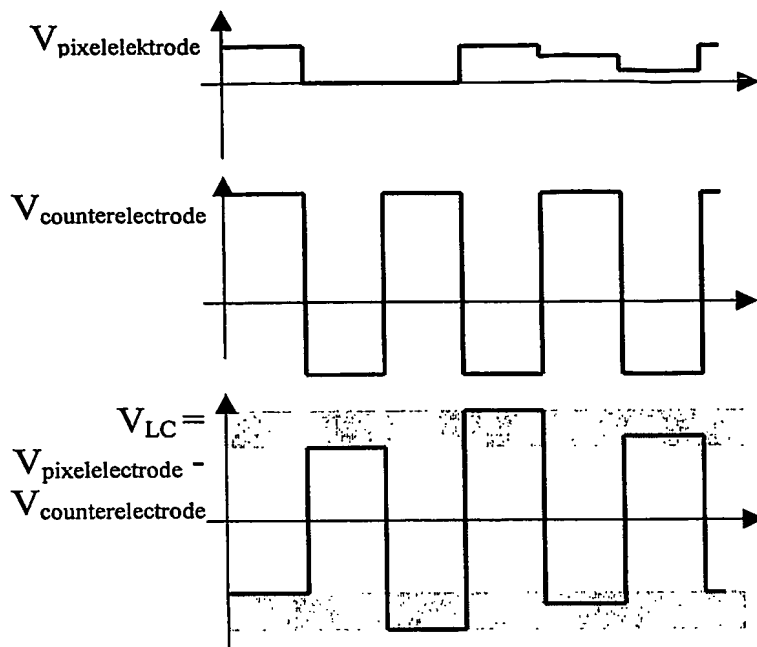


Fig. 9

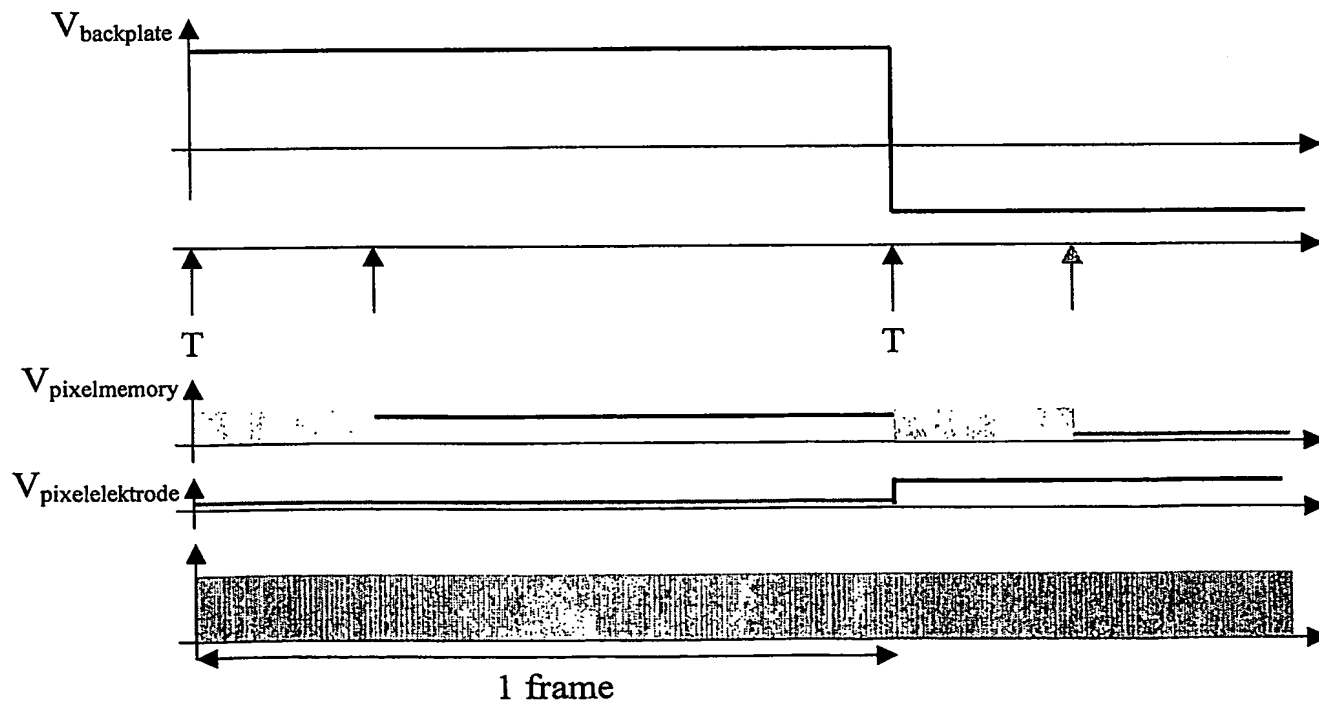


Fig. 10

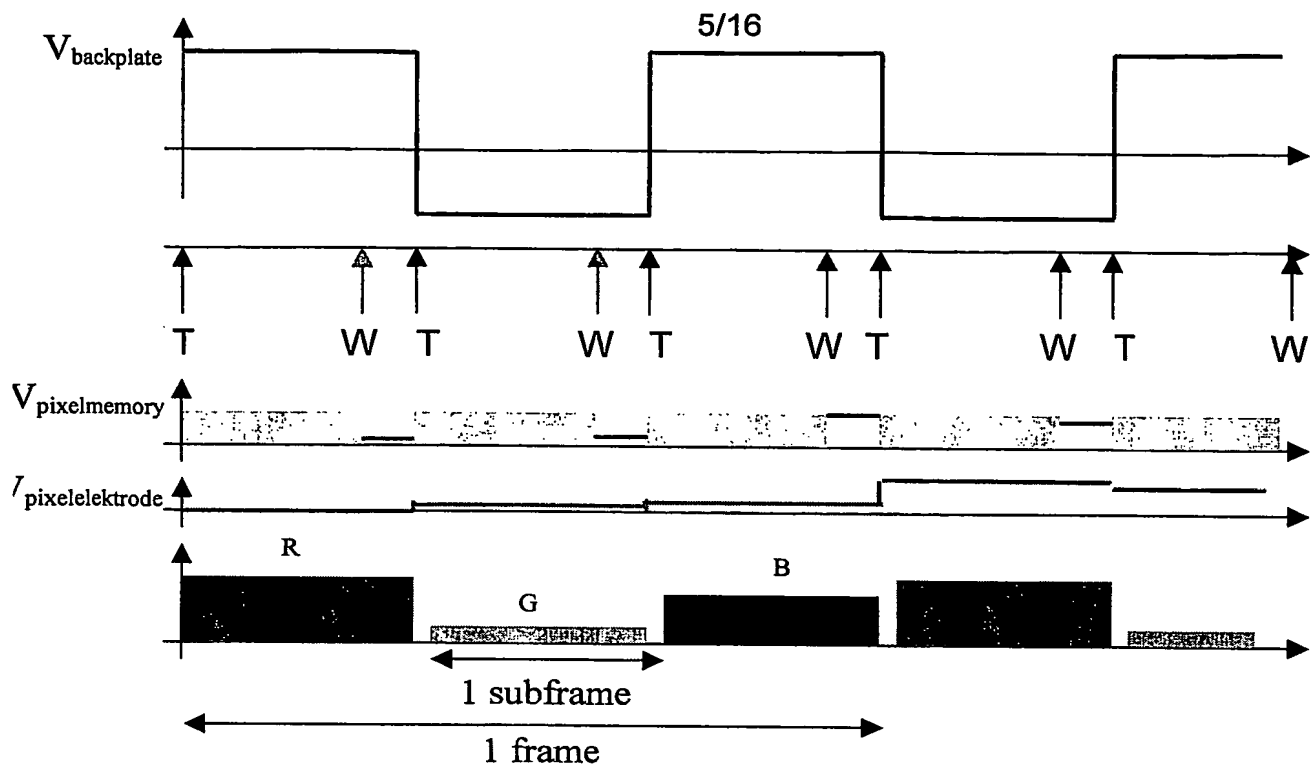


Fig. 11

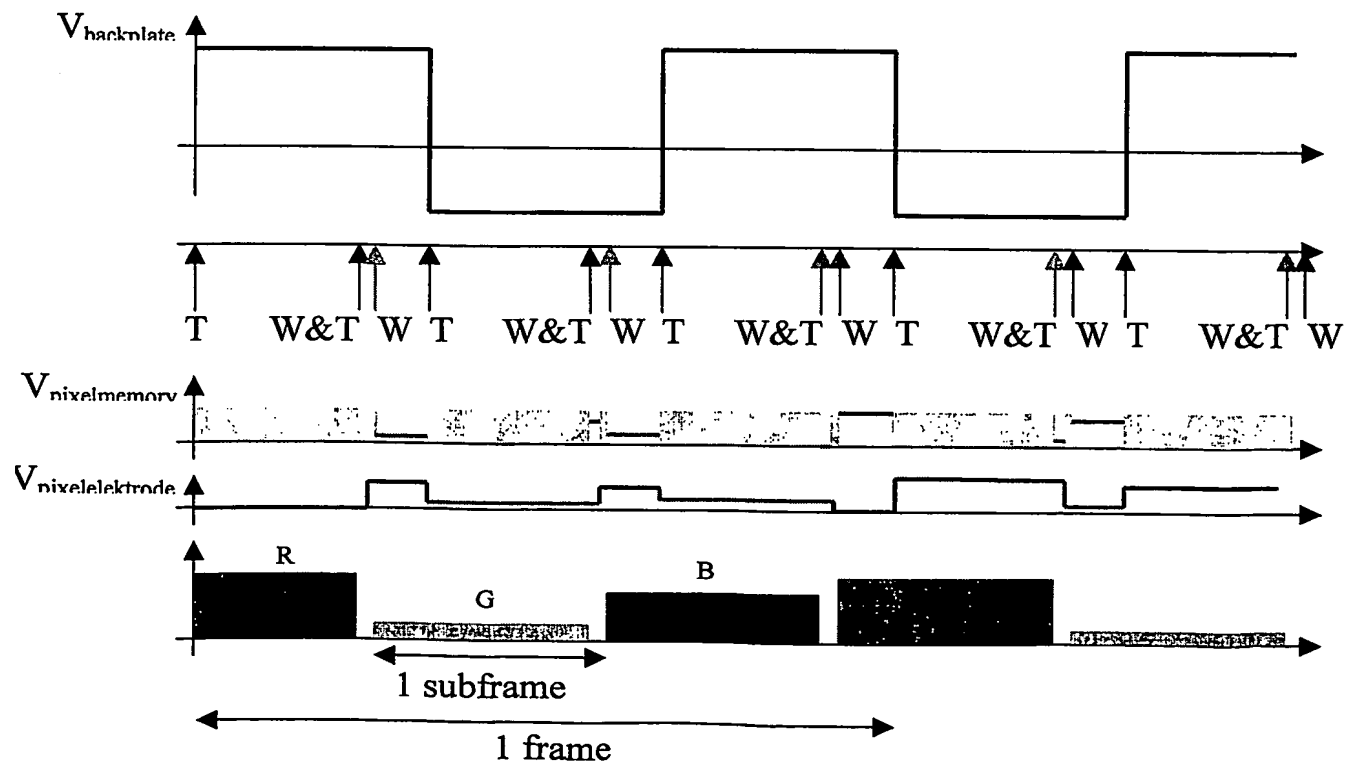


Fig. 12

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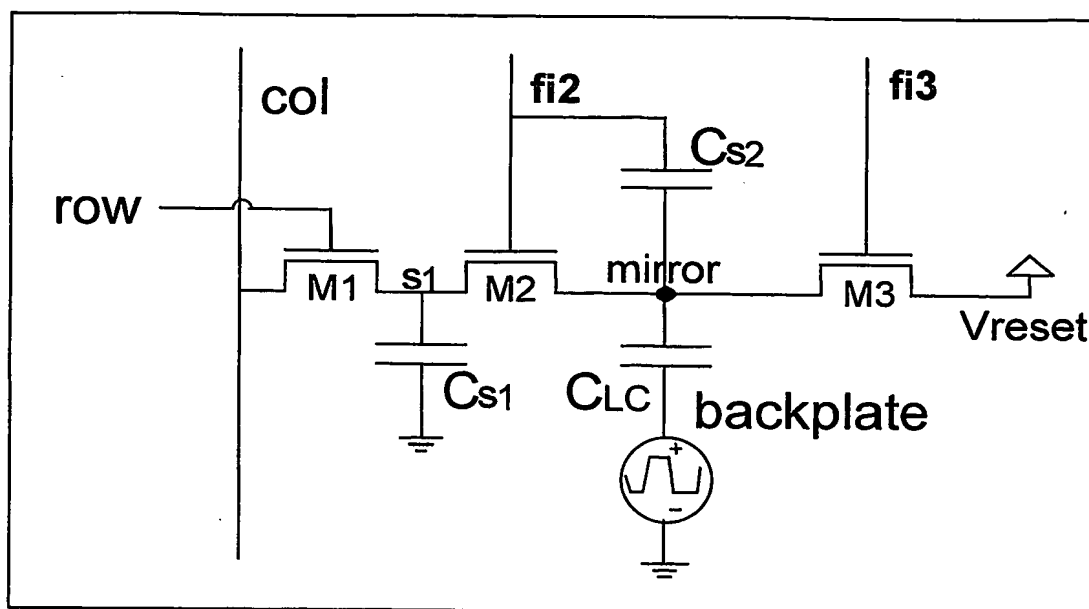


Fig. 13

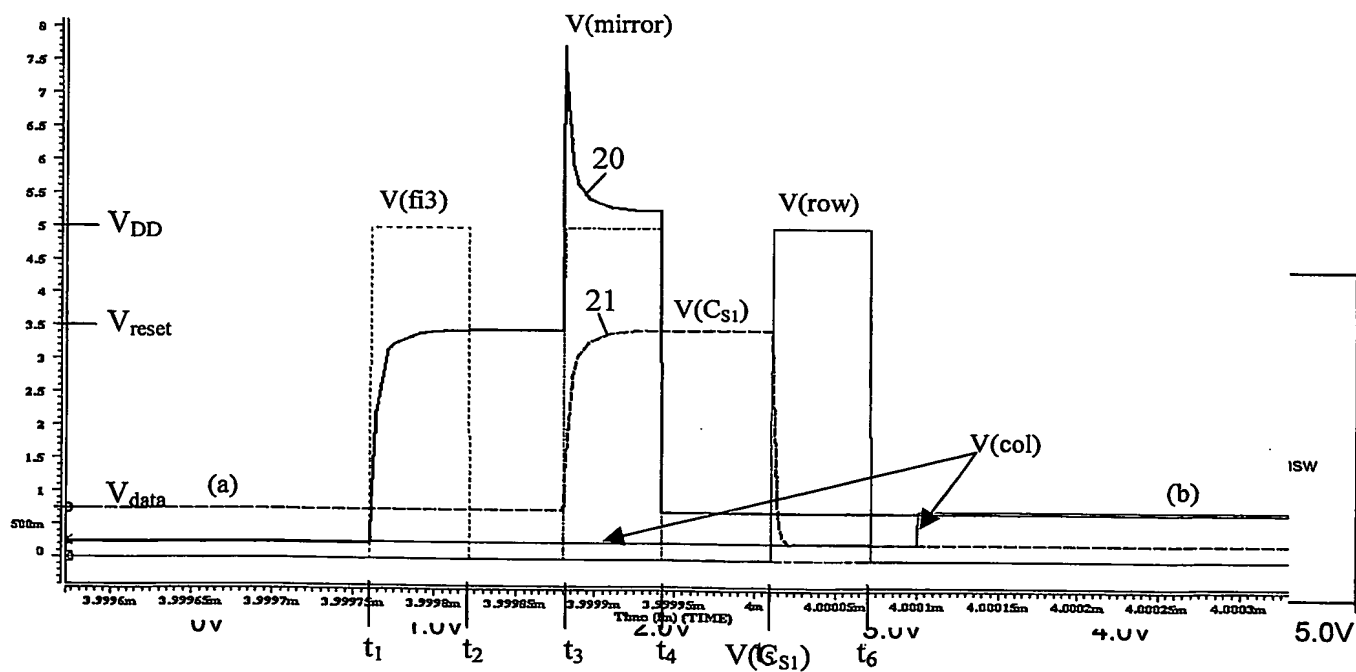


Fig. 14

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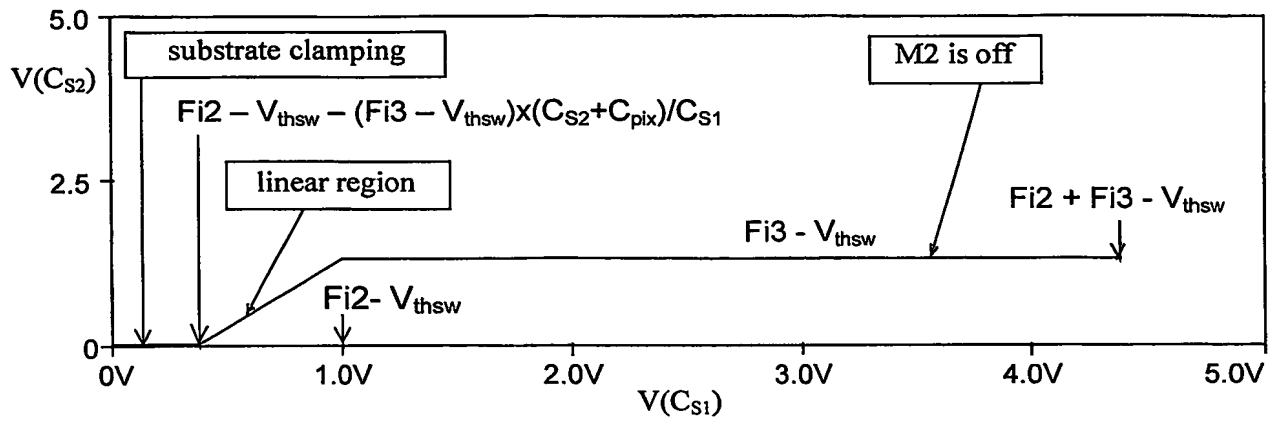


Fig. 15

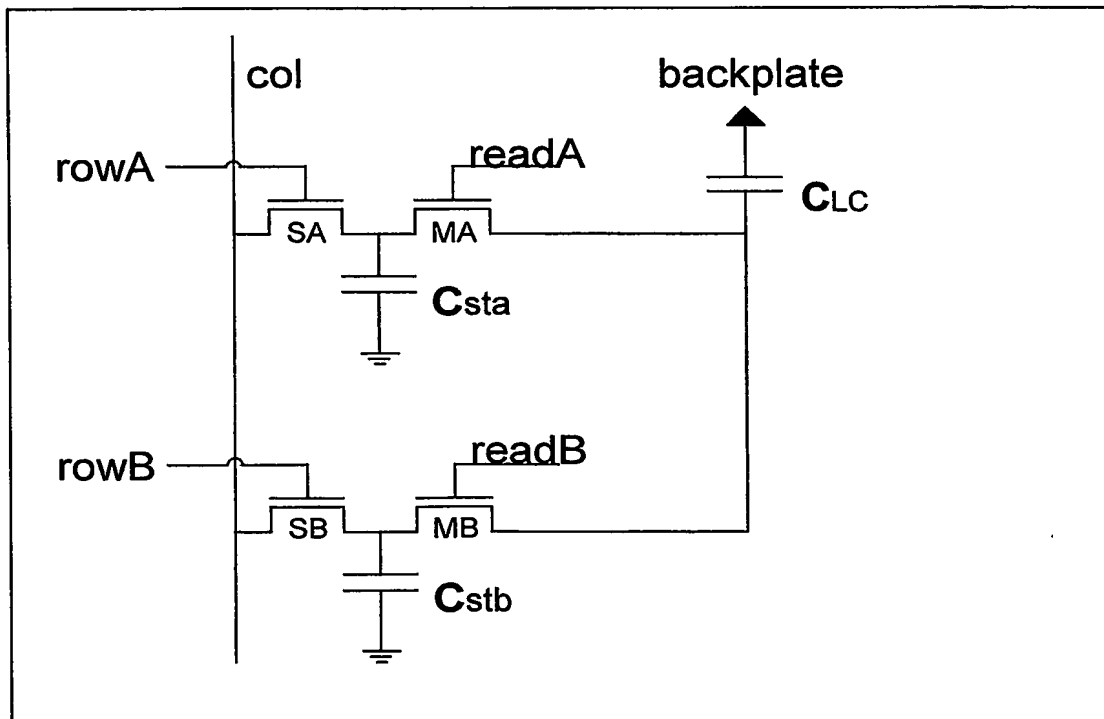


Fig. 16

The schematic diagram illustrates a 4T1C1D1 circuit. It features four NMOS transistors (M9, M11, M13, M14) and two PMOS transistors (M10, M12). The circuit is powered by a 5V supply (V1) and includes a backplate connected to ground. Capacitors C5, C8, and CLC are used for signal conditioning. The input signals are labeled MbreakND. The output is taken from the node between M13 and M14.

Fig. 18

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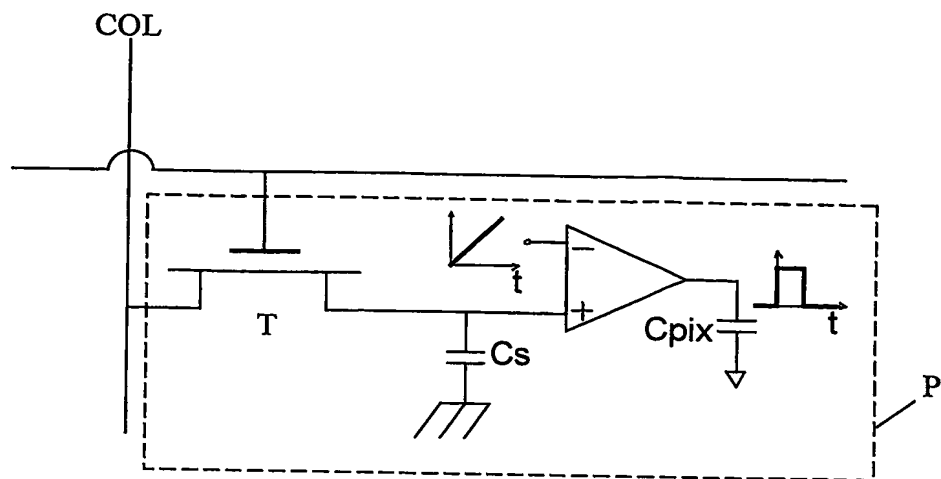


Fig. 19

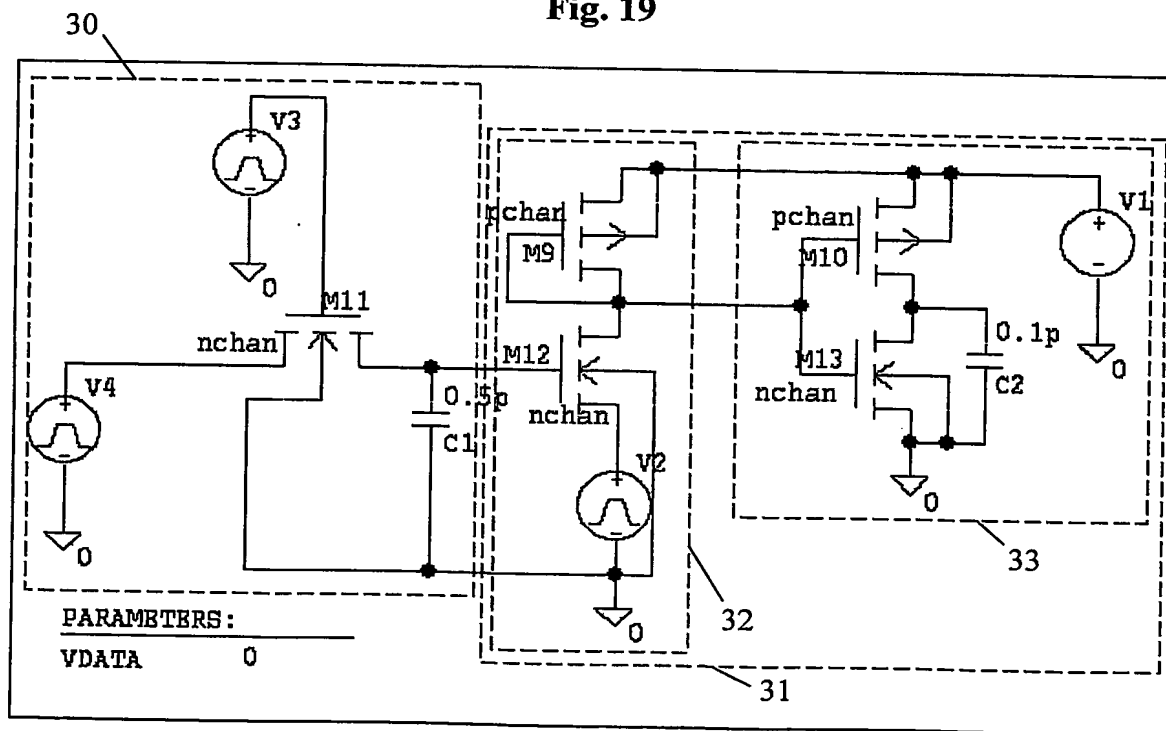


Fig. 20(a)

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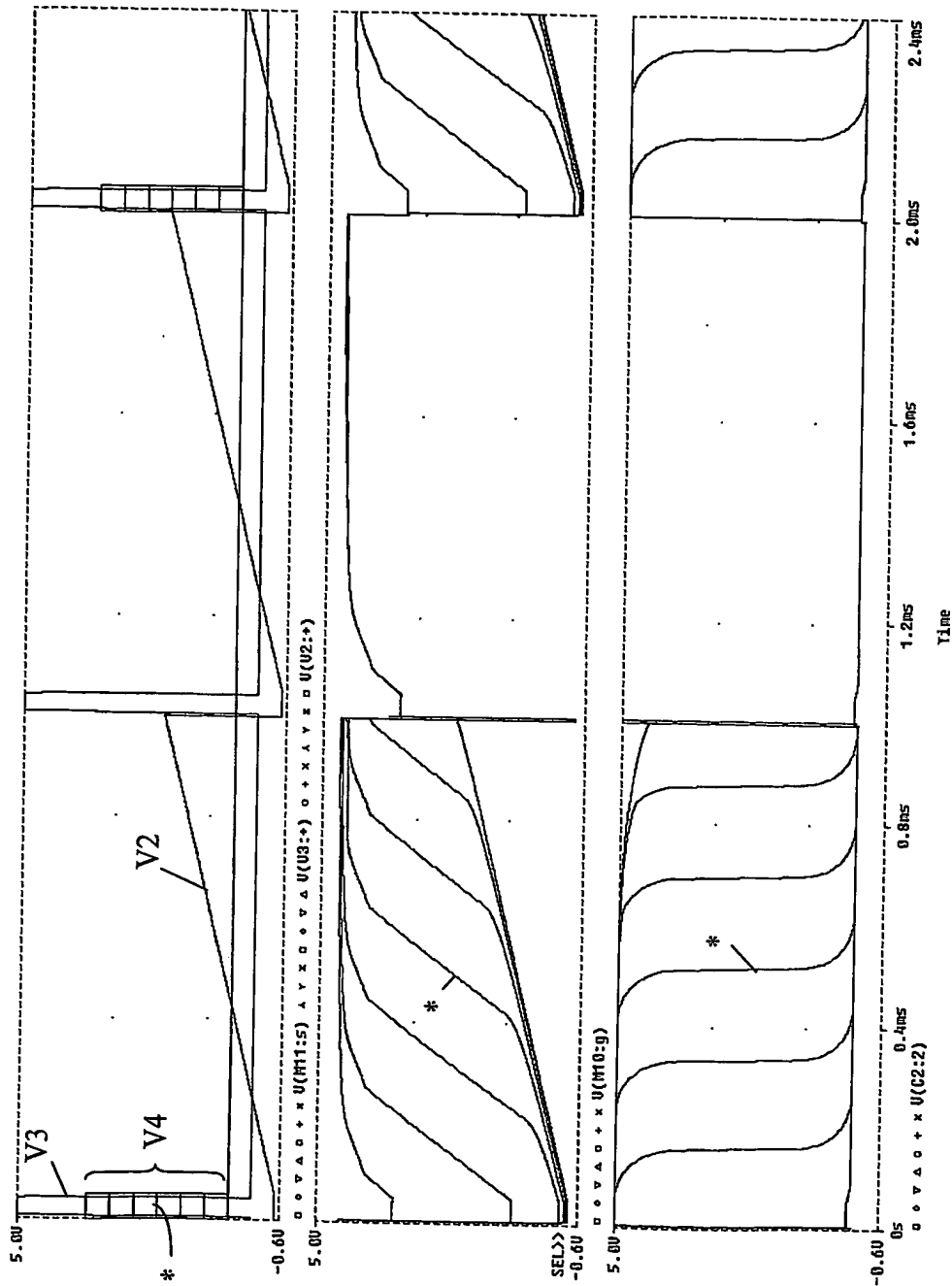


Fig. 20(b)

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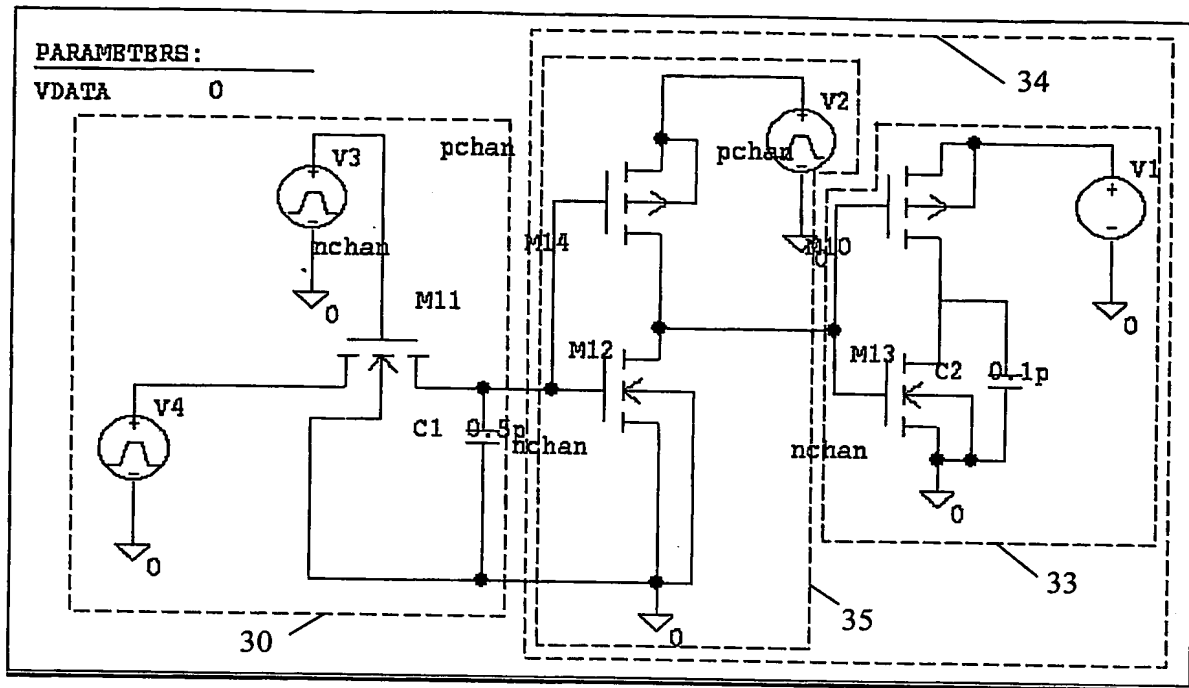


Fig. 21(a)

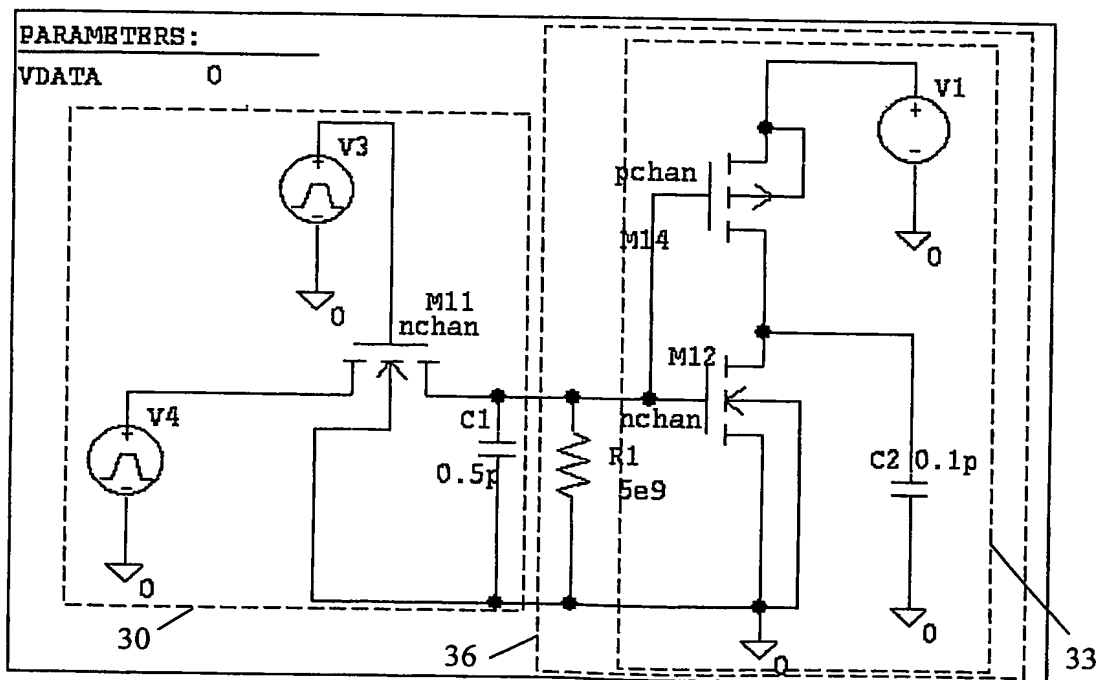


Fig. 22(a)

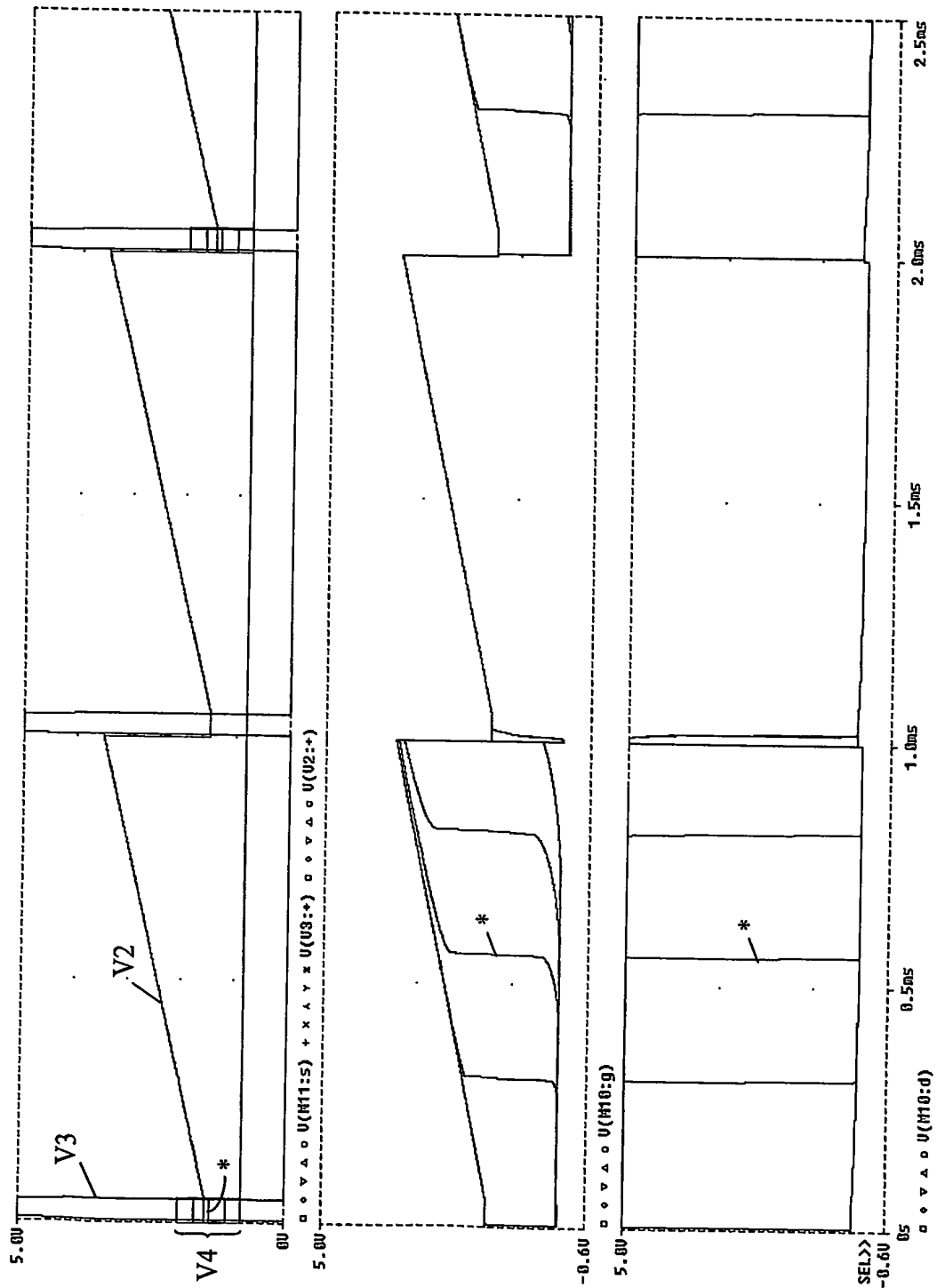


Fig. 21(b)

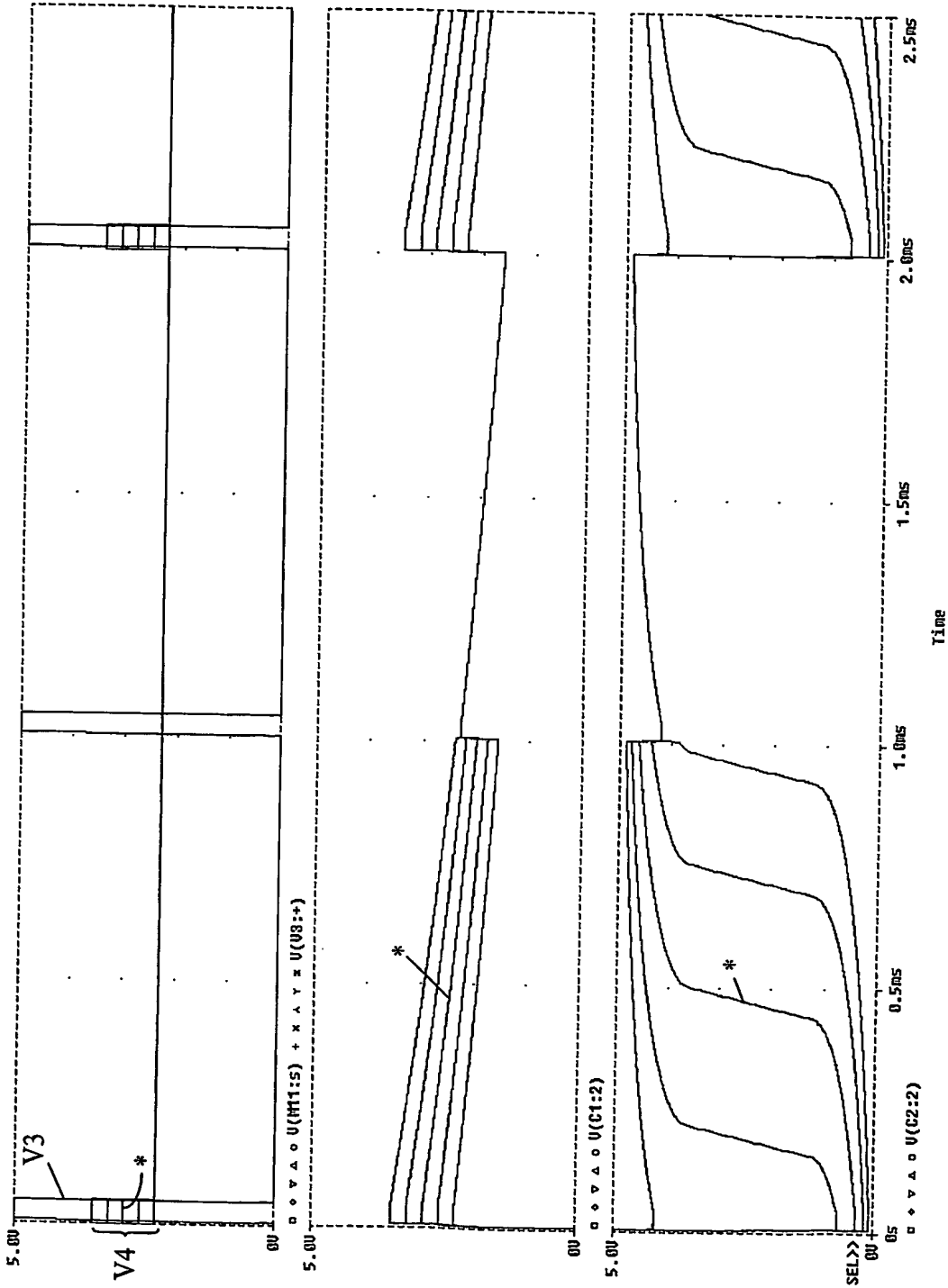


Fig. 22(b)



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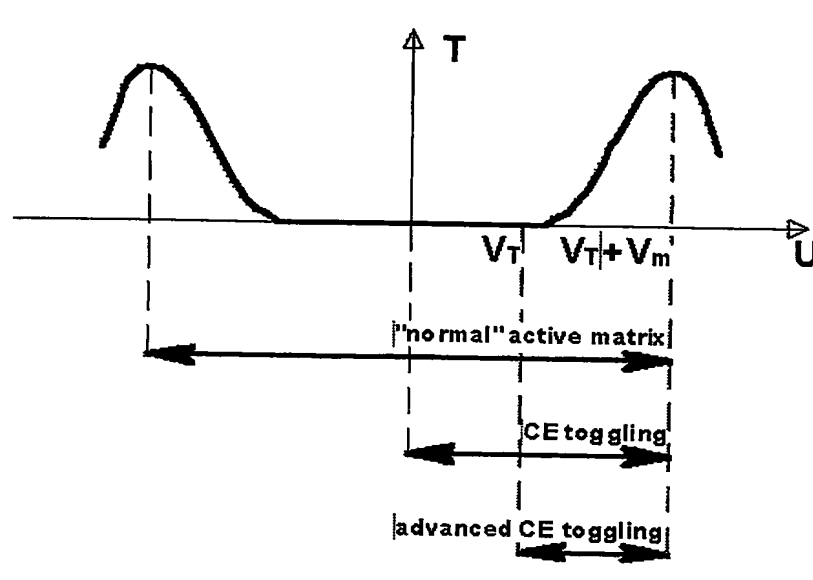


Fig. 25

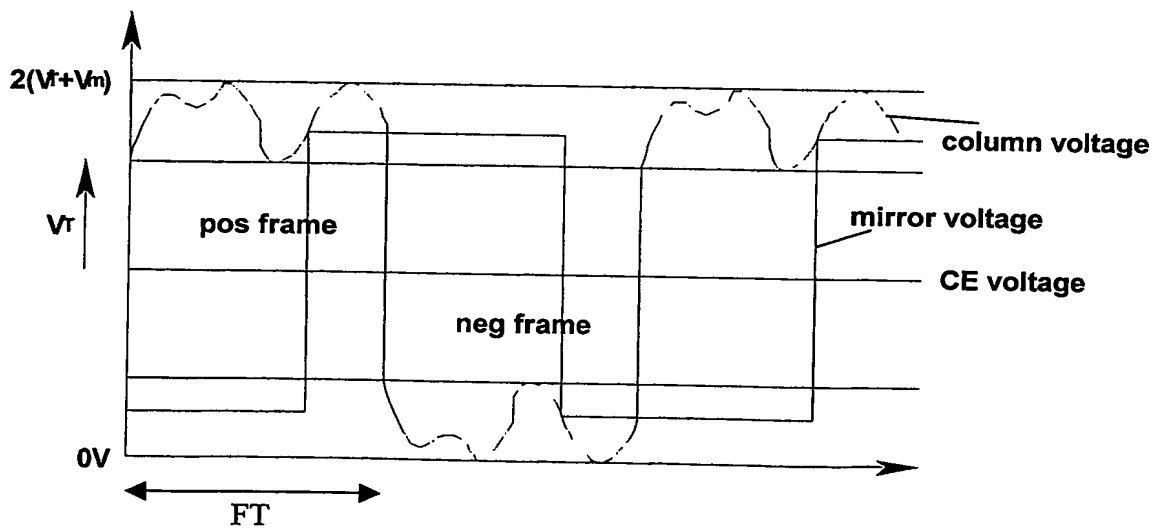


Fig. 26

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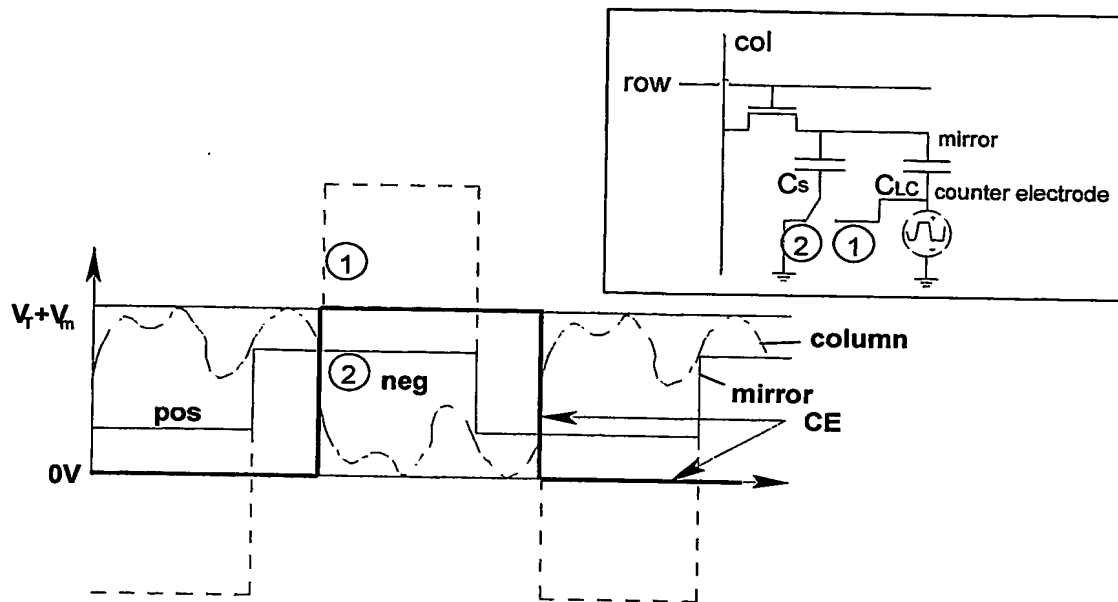


Fig. 27

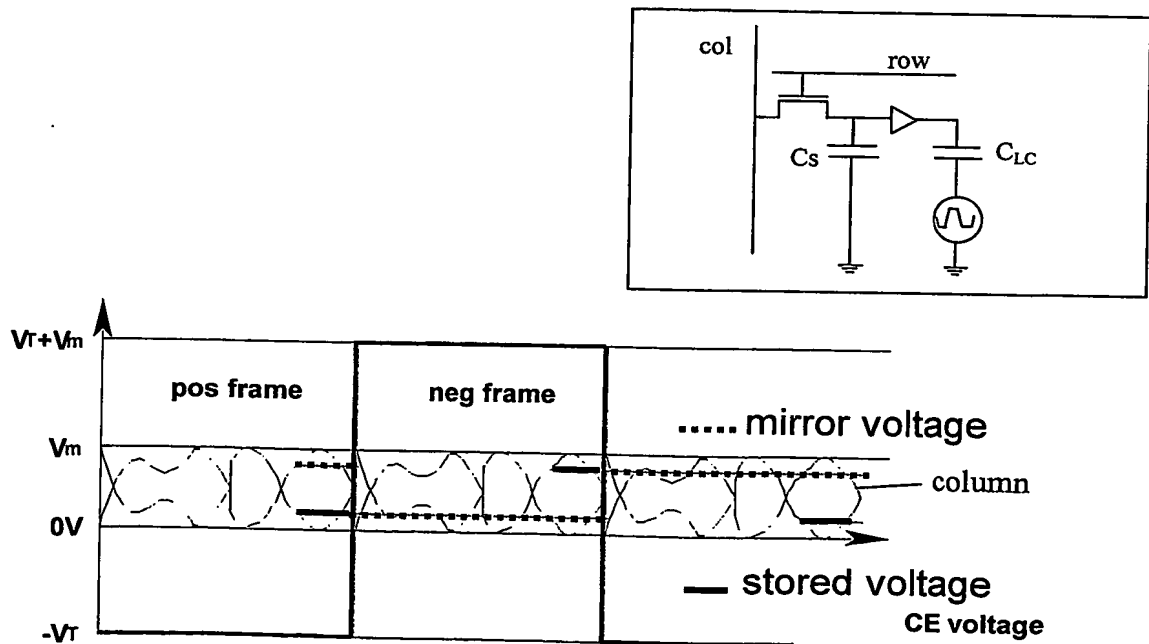


Fig. 28

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